CLAIMS

1. A semiconductor memory device comprising:

a plurality of memory cells each having a source terminal and a drain terminal and a ferroelectric capacitor having a first terminal connected to said source terminal, wherein said plurality of memory cells are connected in series, and one or more selected transistors connected to at least one terminal of said series connected memory cells to constitute a memory cell block, said memory cell block having one terminal connected to a bitline and another terminal connected to a plate electrode, and

wherein two memory cell blocks, which are respectively connected to two bit lines forming a bit line pair and also connected to the same word line, are respectively connected to a first plate electrode and a second plate electrode.

2. A semiconductor memory device according to claim 1, wherein a gate electrode of said transistor is connected to said word lines, and a predetermined number of said memory cell blocks are arranged in a word-line direction to constitute a cell block unit; said first plate electrode and second plate electrode are connected to said memory cell blocks of said cell block unit alternately for every one or for every two memory cell blocks.

3. A semiconductor memory device according to

claim 2, wherein said first and second plate electrodes are respectively connected to two memory cell blocks which are connected to the same bit line.

4. A semiconductor memory device comprising:

a plurality of memory cells each having a source terminal and a drain terminal and a ferroelectric capacitor having a first terminal connected to said source terminal, wherein said plurality of memory cells are connected in series, and one or more selected transistors connected to at least one terminal of said series connected memory cells to constitute a memory cell block, said memory cell block having one terminal connected to a bitline and another terminal connected to a plate electrode, and

wherein a wiring of said plate electrode is formed by the same metal wiring layer such as Al and Cu that constitutes a wiring for connecting said cell transistor and said ferroelectric capacitor of said memory cell.

5. A semiconductor device comprising:

a plurality of memory cells each having a source terminal and a drain terminal and a ferroelectric capacitor having a first terminal connected to said source terminal and a second terminal connected to said drain terminal, and a gate electrode of said cell transistor connected to a word line, wherein said plurality of memory cells are connected in series, and

one or more selected transistors connected to at least one terminal of said series connected memory cells to constitute a memory cell block, said memory cell block having one terminal connected to a bitline and another terminal connected to a plate electrode, and

wherein a metal wiring layer connected with said plate electrode via a contact hole is the same layer as metal wiring layer connected with said word line via a contact hole with predetermined interval.

6. A semiconductor memory device comprising:

a plurality of memory cells each having a source terminal and a drain terminal and a ferroelectric capacitor having a first terminal connected to said source terminal, wherein said plurality of memory cells are connected in series, and one or more selected transistors connected to at least one terminal of said series connected memory cells to constitute a memory cell block, said memory cell block having one terminal connected to a bitline and another terminal connected to a plate electrode, and

wherein a driving circuit for driving said plate electrode is placed in a bit line direction for every one or for every two memory cell blocks.

7. A semiconductor memory device comprising:

a plurality of memory cells each having a first transistor having a first source terminal and a first drain terminal and a ferroelectric capacitor having a

first terminal connected to said firs source terminal and a second terminal connected to said first drain terminal, wherein said plurality of memory cells are connected in series; and a dummy cell having a second transistor having a second source terminal and a second drain terminal and a ferroelectric capacitor or paraelectric capacitor having a third terminal connected to said second source terminal and a fourth terminal connected to said second drain terminal.